Examination (SS 2020)
Communication Systems and Protocols

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Exam: Communication Systems and Protocols
Date: July 28, 2020

Participant:
Matr. №:
ID:

Lecure hall:
Seat №:

The following rules apply:

- The writing time of the examination is 120 minutes.
- No examination aids are permitted, except for
  - one double-sided DIN-A4 sheet of hand-written notes,
  - a non-programmable calculator and
  - a dictionary.
- Answers have to be provided in English.
- Use **permanent ink** only. The usage of pencils or red color is prohibited.
- You are not permitted to use your own writing paper.
- Please do not write on the back sides of the sheets.
- Additional solution sheets are available from the examination supervisors.
  - Make sure that you label all such sheets with your matriculation number.
  - Each additional solution sheet needs to be assigned to exactly one task.

The examination comprises **28 sheets**.

Task 1: Physical Basics

Task 1.1: Sampling and A/D conversion

A) In the figure below, give the four classes of signals which exist in communication channels. Indicate them below the coordinate systems. Then transform the signal shown in gray into these signal classes using the grid provided where applicable.

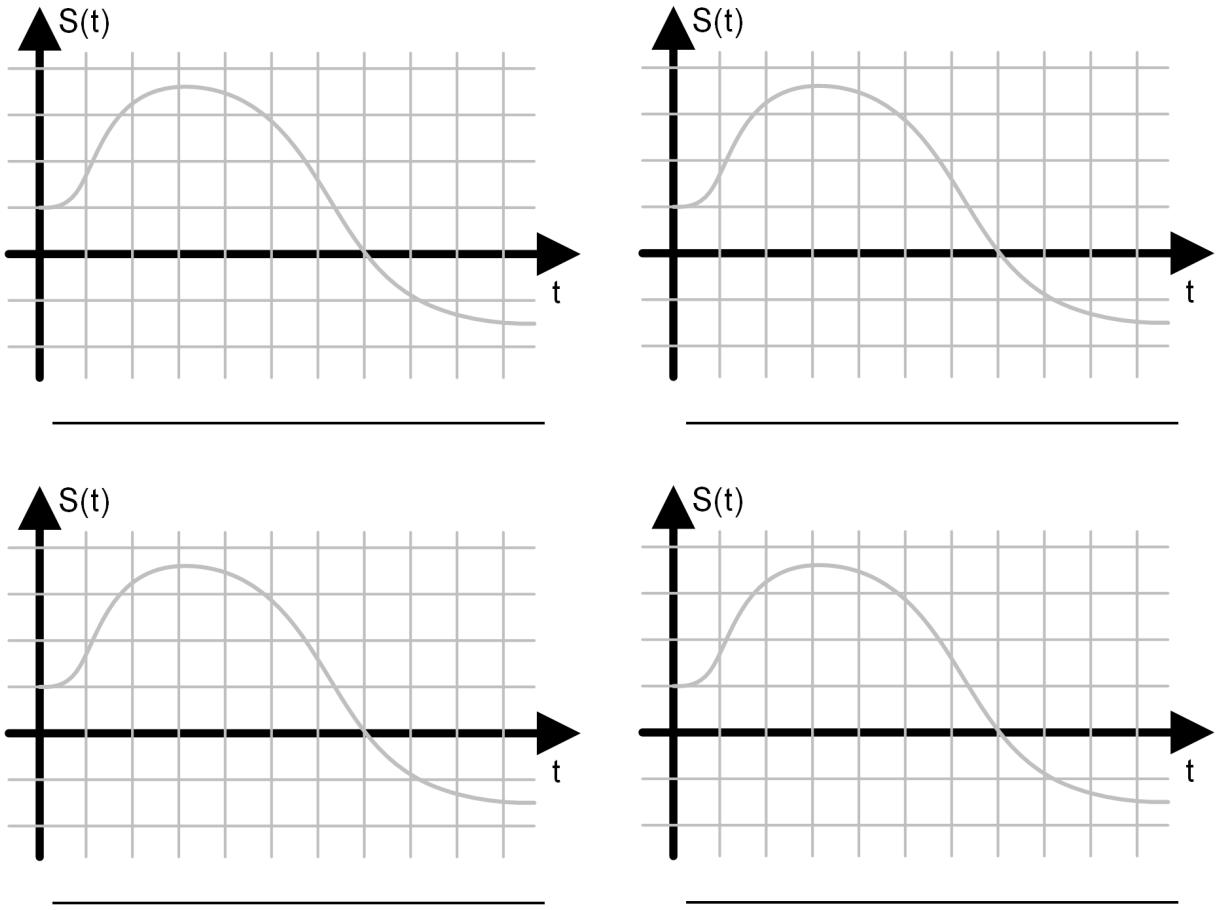


Figure 1.1: Transformation of signals between signal classes

Task 1.2: Drivers

A) Insert the logic level (HIGH/1, LOW/0) of the output and the state of the transistors (conducts/on, blocks/off) into the table according to the input configuration x_1 and x_2 at the standard TTL output driver.

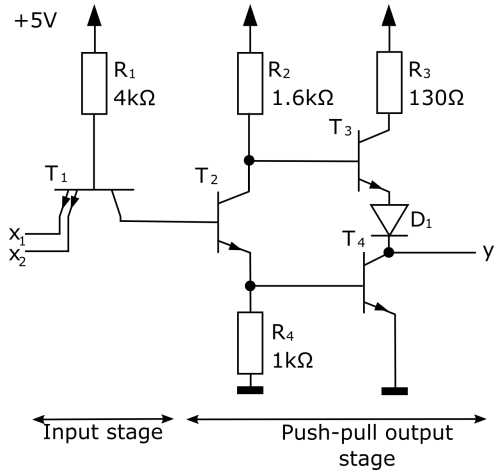


Figure 1.2: TTL output driver

x_1	x_2	T_1	T_2	T_3	T_4	y
1	1					
1	0					
0	1					
0	0					

B) List two advantages of using TTL drivers over open-collector drivers.

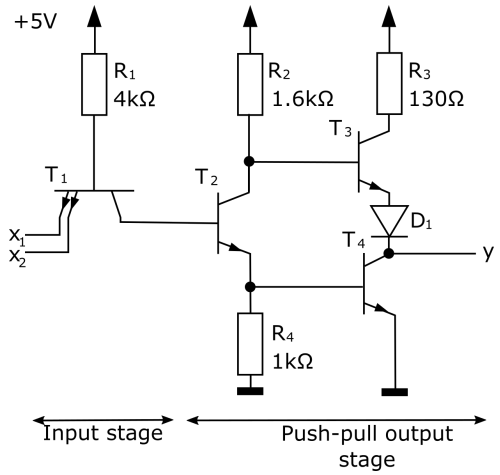


Figure 1.3: TTL output driver

C) How would it be possible to overcome the disadvantage of possible short circuits of a TTL driver? Which part of the TTL driver needs to be modified? Modify Figure 1.3 to get the solution **and** describe the purpose of the adjustments made.

Task 1.3: Signaling

A) Explain the concepts of single-ended signalling and differential signalling. Which differences are there concerning signal paths/lines and concerning the voltages on these lines?

Task 1.4: Reflections on wires

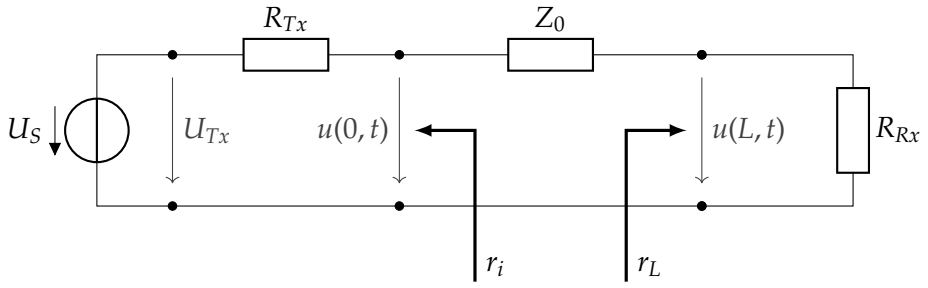


Figure 1.4: Test setup

Figure 1.4 shows the equivalent circuit diagram of an ideal (lossless) transmission line: A transmitter having output impedance R_{Tx} is connected to a receiver with the input impedance R_{Rx} using a long cable.
$R_{Tx} = 90\,\Omega$ and $R_{Rx} = 20\,\Omega$. The signal line is characterized by $Z_0 = 60\,\Omega$.

A) Calculate the value of the reflection factors r_i and r_L and give the formula how to calculate them.

B) Figure 1.5 (next page) shows multiple signal diagrams (A, B, C, D) as seen when the voltage source switches from 0 V to U_S. For this scenario assume $r_i = -0.5$ and $r_L = 0.2$. Which diagram matches the situation described above in this task?

C) For correct termination of the line at the receiving end, an additional resistor R_S shall be added in series to R_{Rx}. Calculate the value of R_S and give the generic formula.

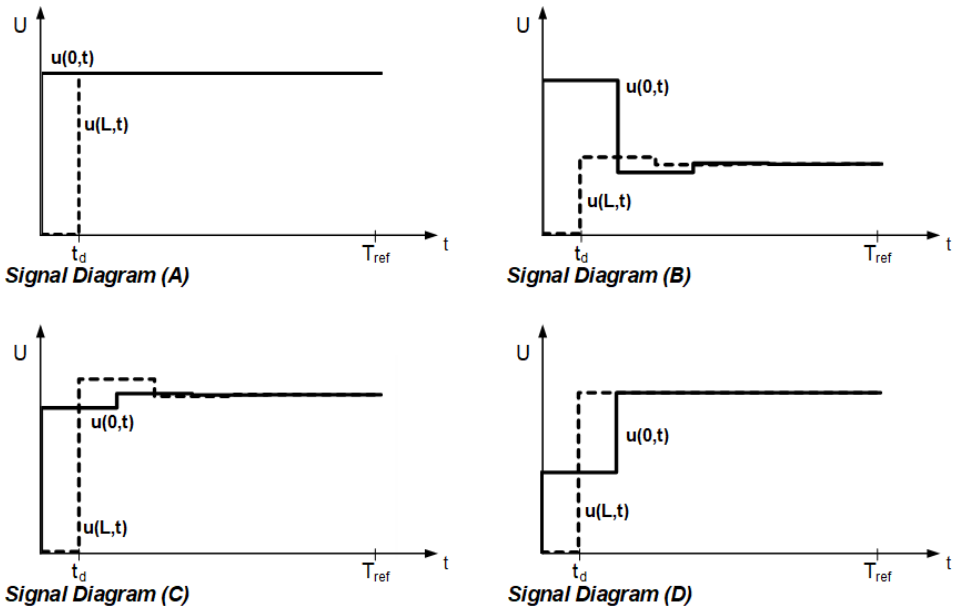


Figure 1.5: Voltages on signal line

D) In this task, the voltages on the line have completely settled (steady state). An ideal voltage source is assumed as transmitter, i.e. $R_{Tx} = 0\,\Omega$.
For the transmission line, a coaxial cable of $L = 90$ m length is used which has an attenuation of 3 dB (non-ideal case). The transmitter and receiver are LVCMOS components, where the transmitter's output signal has an high-voltage of $U_{Tx} = 2.5\,\text{V}$ and the receiver requires a minimum voltage of $U_{Rx,min} = 2\,\text{V}$ for interpreting it as a high level.
An amplifier should be added at the receiver side in order to allow the receiver to properly receive the signal.
What is the high-voltage seen before the amplifier? Which minimum gain G_{min} (in dB) is needed to allow the receiver to properly receive the signal?

Task 2: Modulation and Multiplexing

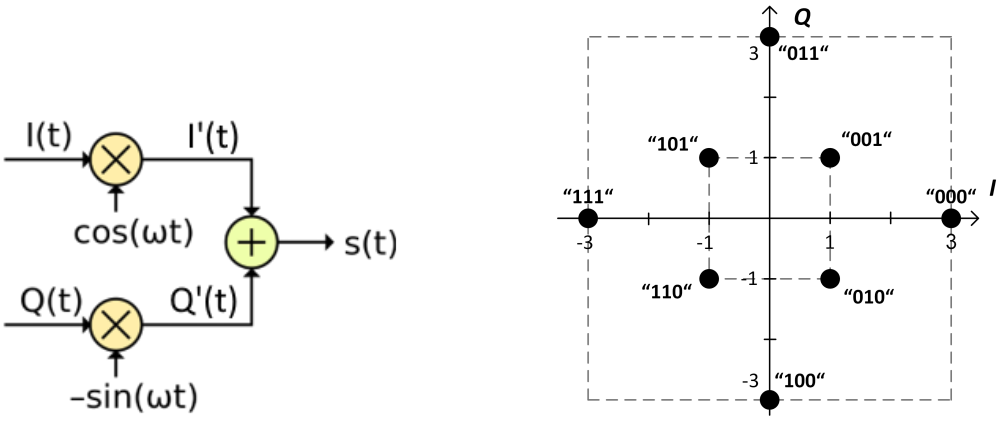
Task 2.1: Modulation

A) Explain the difference between relative and absolute Phase Shift Keying (PSK).

B) Apart from the already mentioned PSK, name the two other digital modulation schemes introduced in the lecture that only modulate one quantity. Give a short explanation of the working principle of each of those.

C) How are the orthogonal signal components used in QAM called? Give the full names.

Figure 2.1a shows a QAM modulator as it has been introduced in the lecture. In the following tasks, you will derive the internal signals and ultimately the input data stream from the signal *s(t)*. Figure 2.1b shows the 8-QAM scheme used for the symbol mapping and the symbol period is double the carrier wave period.



(a) QAM Block Diagram

(b) Constellation Diagram of an 8-QAM scheme

Figure 2.1: Information about the used QAM Scheme

D) Figure 2.2 shows the I component modulated signal $I'(t)$. Derive the I component symbol amplitudes $I(t)$.

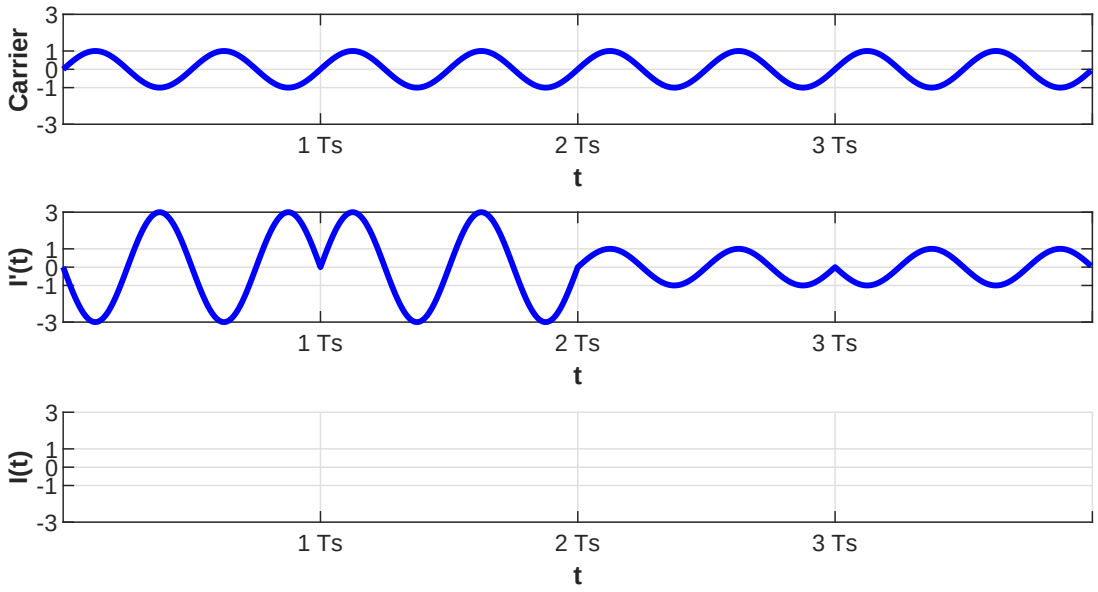


Figure 2.2: I Component Signal

E) Figure 2.3 shows the modulated Q component signal $Q'(t)$. Derive the Q component symbol amplitudes $Q(t)$.

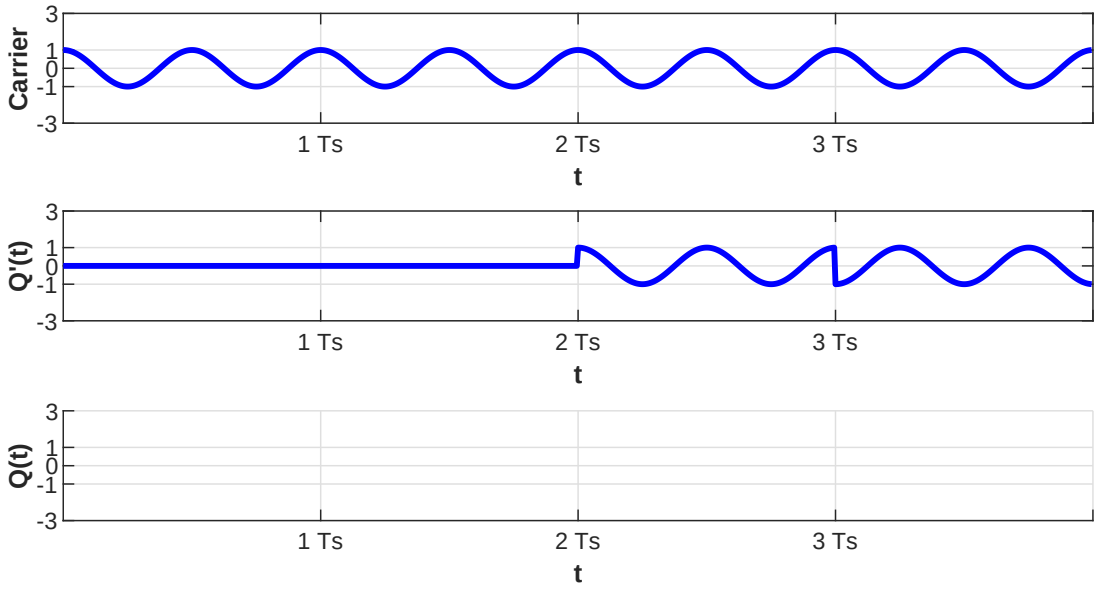


Figure 2.3: Q Component Signal

F) Here, you have been provided with *I'(t)* and *Q'(t)*. Derive the binary data using the waveforms of the I and Q component symbol amplitudes in Figure 2.4 and using Figure 2.1b. Give your answer in Table 2.1.

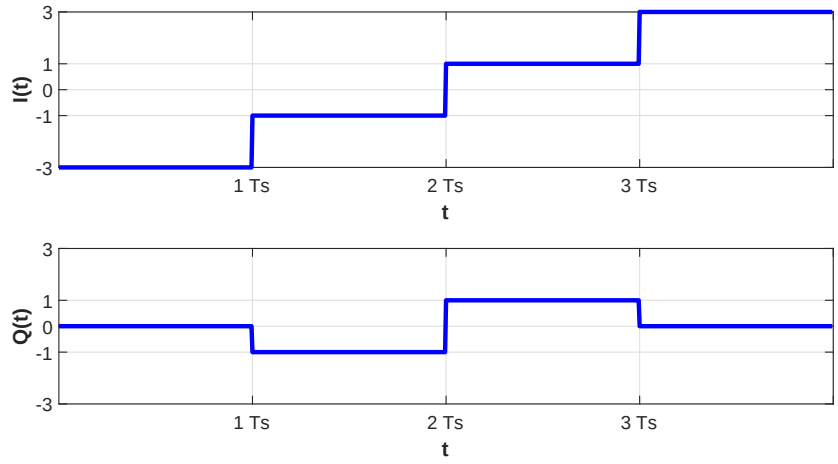


Figure 2.4: *I(t)* and *Q(t)* Component Symbol Amplitudes

	Symbol 0	Symbol 1	Symbol 2	Symbol 3
Start	0	1 Ts	2 Ts	3 Ts
Stop	1 Ts	2 Ts	3 Ts	4 Ts
Data				

Table 2.1: Data which was Modulated into s(t)

Task 2.2: Multiplexing

A) The Walsh functions in Table 2.2 shall be used for the simultaneous data transmission of eight nodes. Complete the blank cells in Table 2.3 with the sending signal for each node.

Sender Node	Function							
0	+1	+1	+1	+1	+1	+1	+1	+1
1	+1	-1	+1	-1	+1	-1	+1	-1
2	+1	+1	-1	-1	+1	+1	-1	-1
3	+1	-1	-1	+1	+1	-1	-1	+1
4	+1	+1	+1	+1	-1	-1	-1	-1
5	+1	-1	+1	-1	-1	+1	-1	+1
6	+1	+1	-1	-1	-1	-1	+1	+1
7	+1	-1	-1	+1	-1	+1	+1	-1

Table 2.2: Walsh Functions for Nodes

Node	Data	Signal to be Sent							
4	"0"								
5	"1"								
6	"0"								
others	"silent"								
Signal on Media									

Table 2.3: Transmission with CDMA

B) Show that Walsh function 6 is orthogonal to function 7. Also give the result of the inner product of Walsh function 7 with itself. The approach must be shown clearly.

Task 3: Media Access

Task 3.1: Carrier Sense Multiple Access/Collision Detection

A bus system of several nodes are using CSMA/CD as arbitration scheme.

A) Is the length of the media related to the duration of sending? Give a short explanation.

B) Name two disadvantages of CSMA/CD in contrast to CSMA/CR. Explain your answers briefly.

C) A signal called JAM signal is used in CSMA/CD. Explain the purpose of this signal and when it is used?

Task 3.2: CSMA/CR

A bus system of four nodes are using CSMA/CR as arbitration scheme and are connected via open collector drivers and a wired-AND connection. Each node has a five Bit identifier and the bus has to cover a maximum distance of 600m.

A) The data format uses a frame with a Start Of Frame bit (SOF) and an identifier with five bits. The identifiers can be taken from Table 3.1. Using Figure 3.1, draw the impulse diagram

Node	Identifier
A	10101
B	10001
C	10110
D	10011

Table 3.1: Identifiers of the nodes

for the arbitration of the single nodes and the signal level of the shared bus line. Which node is granted exclusive access to the bus?

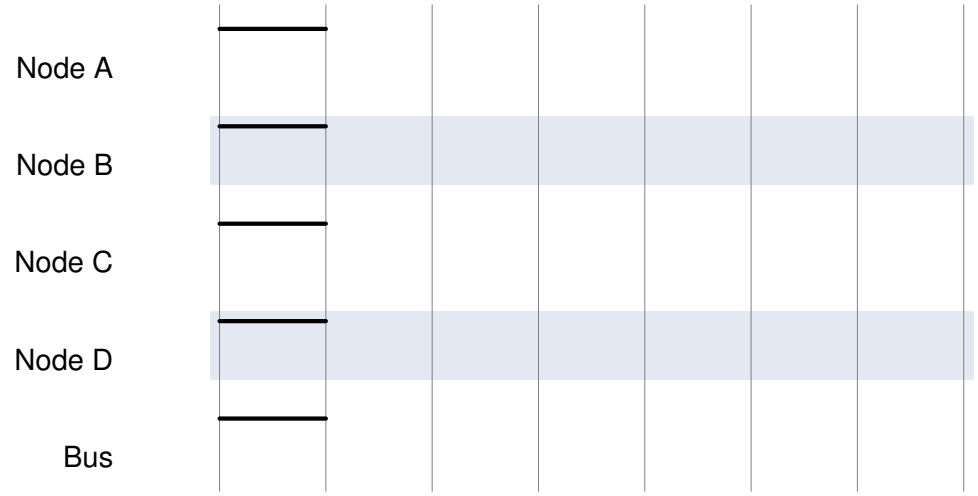


Figure 3.1: Bus Access

B) Which requirements have to be fulfilled in order to guarantee a faultless function of the system? What are the implications for the transmission rate?

C) Arrange the media access schemes CSMA/CR, CSMA/CD and Aloha according to their average channel utilization, start with the lowest channel utilization.

Task 3.3: Arbitration

A) Name one advantage of arbitration compared to static multiplexing schemes like TDMA. Justify your answer briefly.

B) Explain the differences between centralized and decentralized arbitration schemes briefly.

C) A system using polling with a central arbiter is shown in Figure 3.2. An exemplary arbitration cycle of the system is shown in Figure 3.3. Assign the correct signals of Figure 3.2 to the signals shown in the diagram (Figure 3.3). What node is sending data at which point in time? Complete the diagram (Figure 3.3) accordingly.

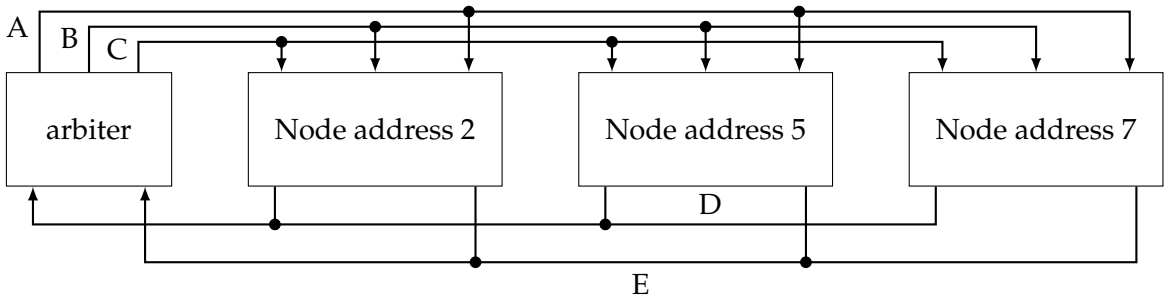


Figure 3.2: Polling

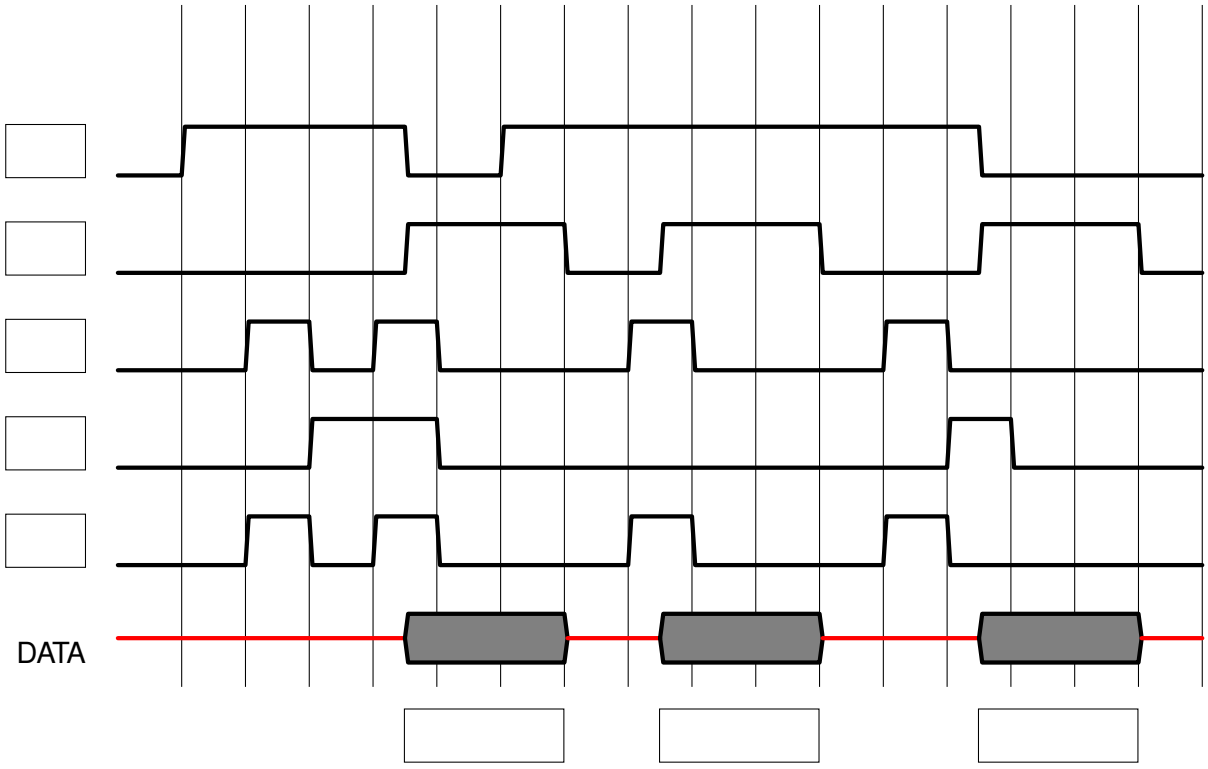


Figure 3.3: Signal flow for Polling

Task 4: Error Protection

Task 4.1: Cyclic Redundancy Check (CRC)

A) Given is a CRC generator polynomial of $G(x) = x^6 + x + 1$. Does the CRC scheme based on $G(x)$ allow a receiver to detect all burst errors of length 7? Justify your answer.

B) Consider a sender that is about to transmit a given message. It uses the CRC generator polynomial $G(x) = x^5 + x^4 + x^2 + 1$ to calculate the corresponding CRC checksum, appends this checksum to the raw message, and finally transmits the bit string

0110 1110 0101 100.

Due to transmission errors, however, the recipient receives the bit string

0110 1101 1111 100.

Is the receiver, who is aware of $G(x)$, able to detect this error? Justify your answer based on the error pattern and the specific error detection capabilities of $G(x)$.

Hint: *Do not perform the calculation that the receiver has to perform to detect errors!*

C) The message "1101 010" shall be protected by a CRC checksum based on the generator polynomial $G(x) = x^5 + x^4 + x^2 + 1$. What are the dividend and the divisor of the arithmetic calculation performed to obtain this checksum? Give them in binary form, i.e., as bit strings.

Hint: *This question does not require you to perform the calculation!*

D) A node receives a CRC-protected message based on the generator polynomial $G(x) = x^2 + 1$, performs the CRC detection scheme and obtains a remainder of "0". What can the node reliably conclude regarding the occurrence of single-bit errors? Justify your answer based on the specific error detection capabilities of $G(x)$.

E) A sender and a receiver have agreed to exchange CRC-protected messages based on the generator polynomial $G(x) = x^3 + x + 1$. Perform the CRC error detection scheme that the receiver carries out for the received bit string "0011 1101 1011 00". Which guarantee does the receiver obtain from the result?

F) Draw the simplified form of the linear feedback shift register with XOR operations implementing the CRC generator polynomial $G(x) = x^{13} + x^7 + x^6 + x^3 + 1$.

G) You are tasked with the development of a system that adds an even parity bit to a given bit string. To do so, you shall reuse a CRC transmission hardware module with a configurable generator polynomial $G(x)$. How do you choose $G(x)$ to meet this requirement?

Task 4.2: Controller Area Network (CAN)

A) Name three error detection mechanisms incorporated into the CAN specification.

B) Consider a CAN node that is "error passive" and, due to a physical hardware defect in its internal logic, recognizes every received CAN message as erroneous. Apart from this issue, it behaves according to specification. It does not transmit any messages by itself, but is connected to a fault-free CAN network in which an infinite stream of messages is exchanged. Which error state will the node eventually end up in? Justify your answer.

C) Consider a CAN network that consists of three CAN nodes. One of these nodes, in the following referred to as the sender, transmits a data frame that is received by the remaining two nodes (see Figure 4.2). During the transmission of exactly one data field bit, a receiver experiences a temporary fault and interferes with the transmission by outputing a dominant bit (visualized by the "↯" symbol). The receiver itself does not detect its own error and, starting from the next bit, continues to behave according to the specification. Complete the empty columns in Figure 4.2 with the signal values that the three CAN nodes transmit in response to this event and determine the resulting bus level for all columns.

Hints: *The general form of a CAN error frame is visualized in Figure 4.1. One column in Figure 4.2 corresponds to one bit duration. All other nodes are fault-free for the entire time.*

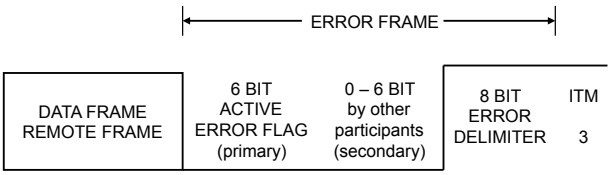


Figure 4.1: Error frame of the CAN protocol

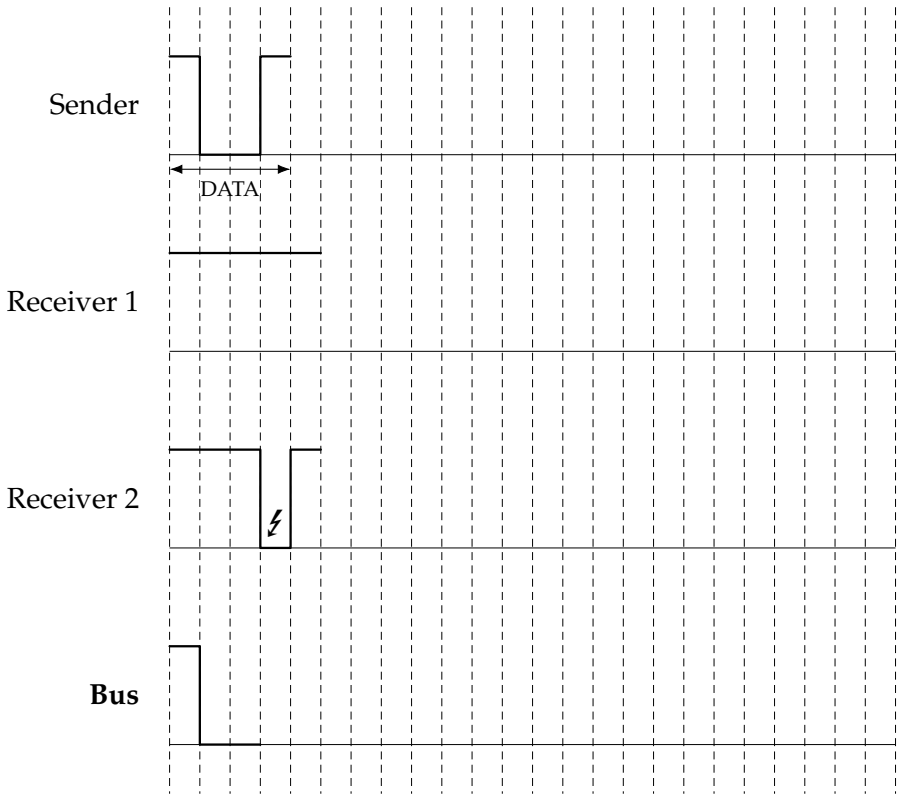


Figure 4.2: Signal sequence diagram of the CAN bus

Task 5: Protocols

Task 5.1: FireWire Arbitration

The FireWire network shown in Figure 5.1 is given.

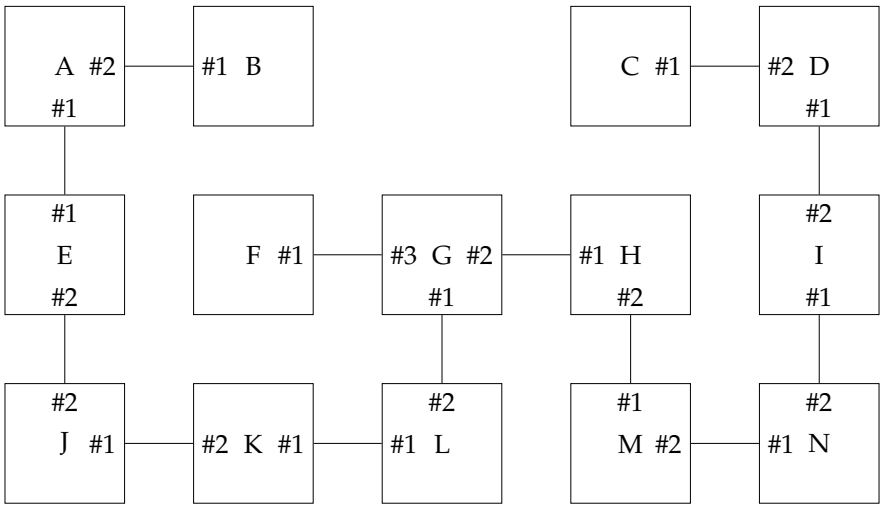


Figure 5.1: FireWire network

A normal FireWire bus cycle should be considered. For simplification, several assumptions should be taken into account:

- A list of nodes wanting to send is given.
- All nodes start requesting the bus at the same time.
- Processing of arbitration requests are done in zero time. There are no delays for propagation of the arbitration decision.
- If a node receives multiple bus requests, it will always forward the request that it receives from the port with the lowest number.

A) The nodes in Figure 5.1 are named using letters from A to N. Which node is the root of the FireWire network?

B) The following nodes in Figure 5.1 request access to the bus: **B, D, G, H, I, L, M**. Determine the order in which the nodes will be granted access to the bus.

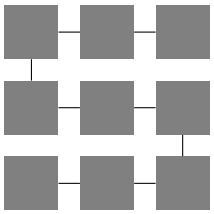
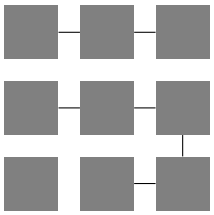
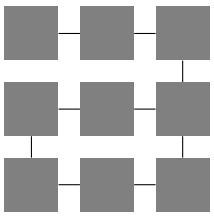
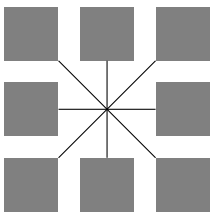
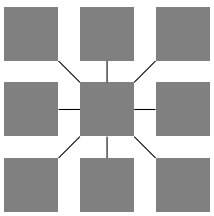
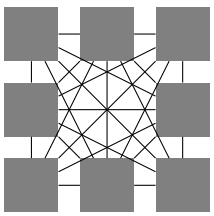
C) Which connections need to be changed in Figure 5.1 in order to get **node L** as root?

D) What happens if two nodes send parent requests to the same node and at the same time during the tree identification process? Does this influence which node becomes the root node? Justify your answer.

E) If the root sends continuously, it would always grant access to the bus. How does FireWire preserve fairness? Explain your answer for multiple sending nodes **and** for only root sending.

Task 5.2: FireWire Structures

A) Different FireWire structures were built during a student laboratory. During the test phase you notice that not all of them are working correctly. State if the FireWire systems shown below are working correctly. If the systems are correct mark the roots. If the FireWire system is not working correctly, give a reason for this.

	Correct	Wrong	Reason
			
			
			
			
			
			

Task 5.3: Serial Peripheral Interface Bus (SPI)

The Serial Peripheral Interface bus (SPI) is a synchronous serial communication bus specification used for short distance communication.

The SPI bus specifies the following logic signals:

- **SCLK**: Serial Clock (output from master).
- **MOSI**: Master Output Slave Input (data output from master).
- **MISO**: Master Input Slave Output (data output from slave).
- **SS**: Slave Select (active low, output from master).

Consider the following protocol options and hints:

- The master selects each slave device with a logic level 0 on the individual select line.
- No waiting period is required between slave select and first clock cycle.
- Slave devices have tri-state outputs so their MISO signal becomes high impedance when the device is not selected.
- During each SPI clock cycle, a full duplex data transmission occurs between master and each slave device.

A) Name one advantage and one disadvantage of using *slave select* signals for accessing a device.

B) Draw the timing diagram for the case that the following data byte (given in binary notation) should be transmitted to a single slave: 11000101_b. As part of the transmission, the slave sends back the data byte: 01100110_b.
Assume the data is captured on the rising edge of the clock and all slaves are unselected at the beginning. Use Figure 5.2.

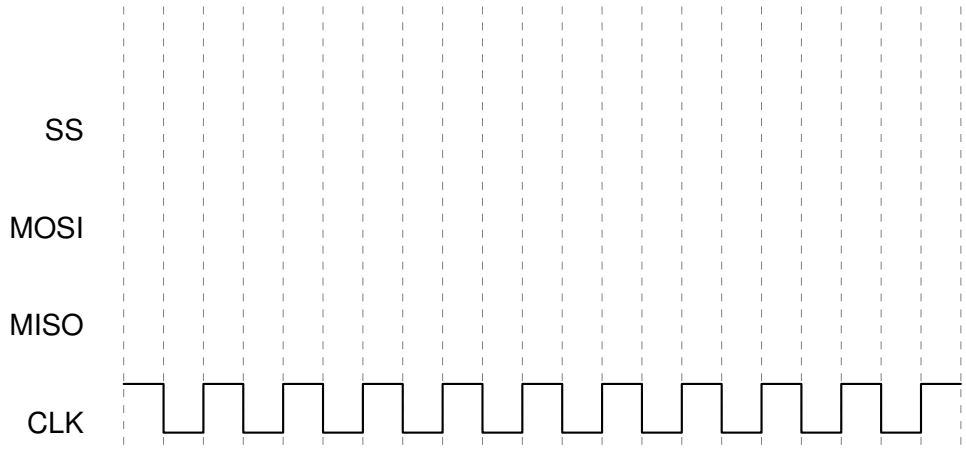


Figure 5.2: SPI full-duplex operation timing diagram

C) Figure 5.3 shows an SPI read operation from a single slave. Add an appropriate SS signal to the diagram and write down the data the master **reads** from the slave in binary notation. Assume the data is captured on the rising edge of the clock and all slaves are unselected at the beginning.

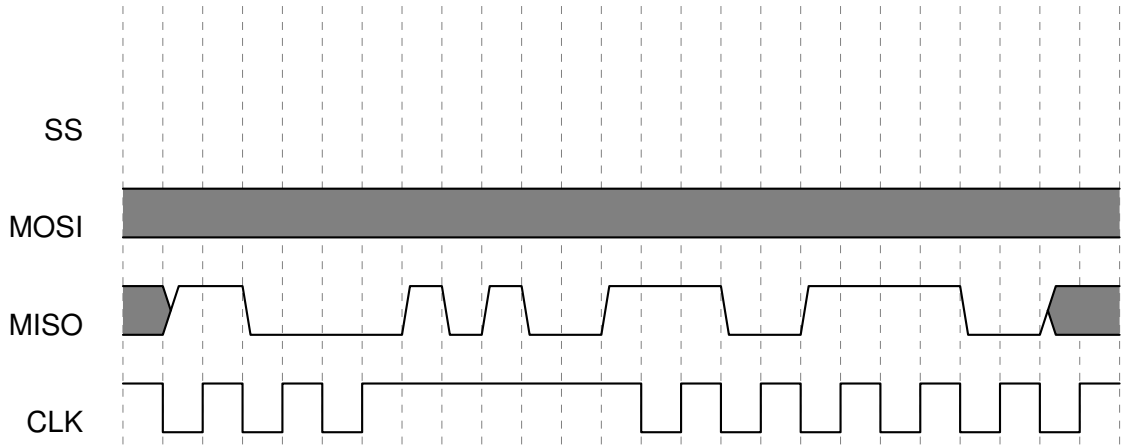


Figure 5.3: SPI read operation timing diagram

Task 6: Routing

Task 6.1: Router and Switching

A) The switch matrix of a router can be implemented using full or reduced crossbars. Describe how both differ in terms of hardware resources and routing capabilities.

B) When using *circuit switching*, packets are divided into flits. Name the three different types of flits and explain the role of each within a circuit-switched connection.

C) Compare *packet switching* and *circuit switching*. Give two advantages for each method.

Task 6.2: Routing

A) Name three optimization goals for a routing algorithm.

B) Explain the difference between source routing and distributed routing. Additionally, give one advantage of each strategy.

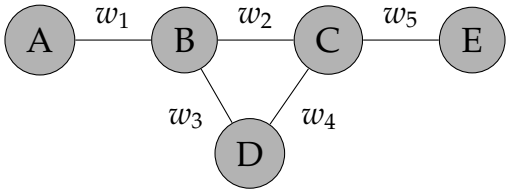


Figure 6.1: A network topology

C) Figure 6.1 shows a network topology with equal weights w_n on every link. Give the number of hops of the route from node A to E using minimal routing. Additionally, describe how the number of hops can change for the same pair if weights are differing and non-minimal routing is used.

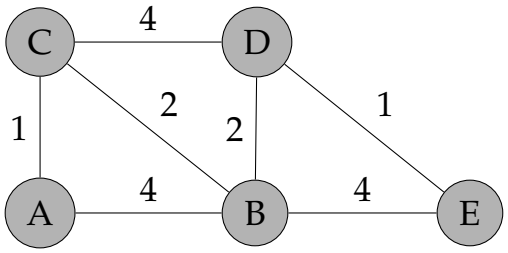


Figure 6.2: Given network topology

D) Figure 6.2 represents a network for which an optimal routing has to be found. The weights represent an abstract metric for traffic present at each connection. With node **E** as the starting point, calculate the paths with the lowest total traffic in the network by using Dijkstra's algorithm. For that write down the order in which nodes are visited in each bracket under the current step and fill out the given tables that encompass the shortest paths after each visitation of a node.

node	step 0 **E**		step 1		step 2		step 3		step 4		step 5	
vertex	dist.	pred.	dist.	pred.	dist.	pred.	dist.	pred.	dist.	pred.	dist.	pred.
A	∞	-										
B	∞	-										
C	∞	-										
D	∞	-										
E	0	E										

Table 6.1: Dijkstra's algorithm

Task 7: Network Topologies

Task 7.1: General Questions

A) Define edge connectivity of network. What is the edge connectivity of a 4x4x4 Torus Network ?

B) Compute the Edge Connectivity and Diameter for 4x4 Torus, 5 node Star, 5 node Ring and 3x2x4 Mesh topologies. All links here are bidirectional. Use the table below.

Topology	Edge Connectivity	Diameter
4x4 Mesh		
5 Node Star		
5 Node Ring		
3x2x4 Mesh		

Table 7.1: Topologies and Metrics

Task 7.2: Congestion Aware Routing

A system was designed which comprised of 23 Processing Tiles and 2 Memory Tiles. The total of 25 Tiles were interconnected using a NoC and the topology used was a 5x5 mesh. Packet switching was used and XY routing was implemented in the routers.

A) Find the path of packets from the source (x,y) = (1,2) to the destination (x,y) = (3,1). In your answer please name all traversed nodes (i.e. their coordinates) in the correct sequence.

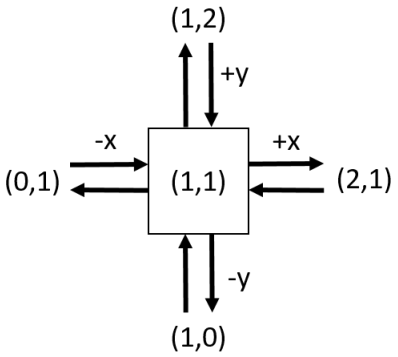


Figure 7.1: Node at (x,y) = (1,1)

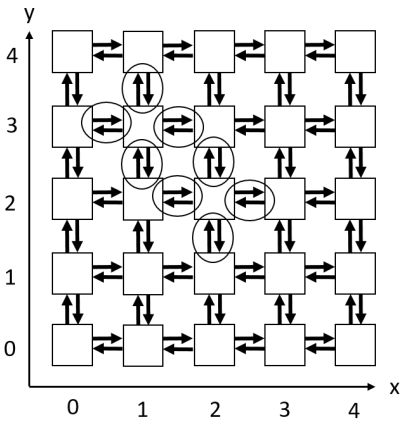


Figure 7.2: 5x5 Mesh network

B) Memory tiles are present at (x,y) = (1,3) and (x,y) = (2,2). Overtime, high traffic around those nodes led to congestion on the links connected to the memory tiles. The congested links are illustrated in Figure 7.2. To solve this issue, XY routing at each router was replaced with a custom adaptive routing algorithm which followed the rules provided below.

Rule1 Try to first route the packet in the X direction towards the destination. Then the Y direction towards the destination. If the chosen link is congested, go to Rule 2

Rule2 Choose among the remaining directions in the decreasing order of priority -y,-x,+y,+x. Use Figure 7.1 as a guide. If link chosen does not exist or is congested, do not select this link and repeat Rule 2

What is the path a packet takes from the source (x,y) = (0,3) to the destination (x,y) = (2,1). In your answer please name all traversed nodes (i.e. their coordinates) in the correct sequence. Mention which of the above mentioned rules you used to go to the next node.

C) Find the path of packets from the source (x,y) = (0,2) to the destination (x,y) = (2,3). In your answer please name all traversed nodes (i.e. their coordinates) in the correct sequence. Mention which of the above mentioned rules you used to go to the next node. Does the packet reach the destinaton ? What do you notice ?